LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1	28/6	Number systems	1	Chalk & Dust		
2	29/6	Base Conversion Methods	1	"		
3	29/6	Complement of Numbers	1	"		
4	1/7	r's complement Subtraction	1	"		
5	5/7	(r-1)'s complement Subtraction	1	"		
6	6/7	BCD Codes	1	"		
7	6/7	Excess-3 Codes	1	"		
8	12/7	Alphanumeric Codes	1	"		
9	13/7	self complement Codes	1	"		
10	13/7	2421 codes	1	"		
11	15/7	gray codes	1	"		
12	19/7	error detection Codes	1	"		
13	20/7	error correction Codes	1	"		
14	20/7	Parity Checking Codes	1	"		
15	22/7	Hamming Codes	1	"		
16	2/8	extra Problems on Code conversions	1	"		
17	3/8	Problems on Subtractions	1	"		
18	3/8	problems on Codes & error detection & correction codes	1	"		
19	5/8	Logic Gates	2	"		
20	9/8	Boolean Theorems	2	"		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
21	10/8	Complements and dual of logic expressions	2	Chalk & Duster		
22	10/8	problems on Logic Gates	2	"		
23	12/8	problems on Boolean Algebra	2	"		
24	16/8	problems on Complements and dual of logic expressions	2	"		
25	17/8	Standard SOP	2	"		
26	17/8	Standard POS	2	"		
27	19/8	Minimization of Logic functions using Theorems	2	"		
28	23/8	problems on standard sum of products	2	"		
29	24/8	problems on standard product of sums	2	"		
30	25/8	problems on SOP & POS	2	"		
31	26/8	Minimization of Logic functions using Theorems	2	"		
32	30/8	Multilevel NAND NAND Realization	2	"		
33	31/8	Multilevel NOR NOR Realization	2	"		
34	31/8	Minimization of switching functions using K-Maps	3	"		
35	2/9	Minimization of switching functions using K-Maps	3	"		
36	6/9	Problems on Minimization of switching functions using K-MAPS	3	"		
37	7/9	Using of K-MAP upto 5 variables	3	"		
38	7/9	problems Minimization of switching functions using 5 variable K-MAPS.	3	"		
39	9/9	Code conversions	3	"		
40	13/9	different codes conversions.	3	"		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
41	14/09	Different types of code convertors	3	Chalk & Duster		
42	14/09	Different types of code convertors	3	"		
43	16/09	Binary Multiplier using K-MAP	3	"		
44	20/09	Binary Multiplier using K-Maps	3	"		
45	21/09	Tabular Minimization	3	"		
46	21/09	Problems on Tabular Minimization	3	"		
47	23/09	Design of Half adder Design of Half Subtractor	4	"		
48	27/09	Design of full adder Design of full Subtractor	4	"		
49	28/09	Applications of full adders	4	"		
50	28/09	4-bit Binary adder 4-bit Binary Subtractor	4	"		
51	30/09	adder-Subtractor circuit.	4	"		
52	4/10	BCD adder circuit Excess-3 adder circuit	4	"		
53	5/10	look a head carry adder circuit	4	"		
54	5/10	Design of decoder	4	"		
55	7/10	Design of Encoder	4	"		
56	11/10	Design of Multiplexer Design of De Multiplexer	4	"		
57	12/10	Design of priority encoder	4	"		
58	12/10	Design of Comparator	4	"		
59	14/10	Design of seven segment display.	4	"		
60	18/10	Classification of Sequential Circuits	5	"		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
61	19/10	flipflops with Truth table & excitation table.	5	Chalk & Duster		
62	19/10	Conversion of flipflop to flipflop.	5	"		
63	21/10	Design of ripple counter	5	"		
64	25/10	Synchronous counter	5	"		
65	26/10	Johnson counters.	5	"		
66	26/10	Ring Counters	5	"		
67	28/10	Design of Buffer Register	5	"		
68	1/11	Control Buffer Register	5	"		
69	2/11	Shift Register	5	"		
70	2/11	Bidirectional shift Register	5	"		
71	4/11	Universal shift Register.	5	"		

4/01/07